Amendments to the Claims

The following listing of the claims will replace all prior versions, and listings of the claims in the application:

Listing of Claims

1. (Currently amended) A PLL clock generator for generating an output signal, of which the frequency is N times (where N is a natural number equal to or greater than 1) as high as that of an input signal, the clock generator comprising:

a frequency divider for counting a clock signal and dividing the frequency of [[a]] the clock signal by N so as to output a frequency-divided clock signal;

a phase comparator for detecting a phase difference between the input signal and the output signal of the frequency divider so as to output a phase difference signal including information representing the phase difference;

a low pass filter for smoothing the phase difference signal;

a voltage-controlled oscillator for generating the clock signal, of which the frequency is determined by the output of the low pass filter, and outputting the clock signal to the frequency divider; ~~and~~

a time width detector for outputting a positive phase difference signal and a negative phase difference signal based on the phase difference signal; and

a phase shifter for advancing the count of the frequency divider if the amplitude of the positive phase difference signal is equal to or greater than a first predetermined value and delaying the count of the frequency divider if the amplitude of the negative phase difference signal is equal to or greater than a second predetermined value ~~controlling the frequency divider in accordance with the phase difference signal~~ so as to change the phase of the output signal of the frequency divider.

2. (Canceled)

3. (Currently amended) The PLL clock generator of claim ~~2~~ 1, wherein the frequency divider, the phase comparator, the low pass filter and the voltage-controlled oscillator together makes up a first feedback loop, and

wherein the frequency divider, the phase shifter and the phase comparator together make up a second feedback loop.

4. (Previously presented) A PLL clock generator of claim 1, further comprising a synchronization detector for determining a synchronization state of a PLL based on the phase difference signal and for instructing the phase shifter to operate in the case of an asynchronous state.

5. (Original) The PLL clock generator of claim 4, wherein the synchronization detector sums up the absolute values of the phase differences, obtained from the phase comparator, for a predetermined period of time and instructs the phase shifter to start to operate if a resultant summation value is equal to or greater than the predetermined value.

6. (Cancelled)

7. (Original) The PLL clock generator of claim 1, further comprising a binarizer for outputting a binary signal by comparing an incoming analog signal with a predetermined signal level,

wherein the input signal is the binary signal.

8. (Original) The PLL clock generator of claim 4, further comprising a binarizer for outputting a binary signal by comparing an incoming analog signal with a predetermined signal level,

wherein the input signal is the binary signal.

9. (Currently amended) An optical disc drive for reading and/or writing data from/on an optical disc with wobbled tracks, the optical disc drive comprising:

an optical head for focusing light on one of the tracks and receiving the light that has been reflected from the track;

a wobble signal generator for generating a wobble signal from an output signal of the optical head; and

a PLL clock generator for receiving the wobble signal and generating an output signal, of which the frequency is N times (where N is a natural number equal to or greater than 1),

wherein the PLL clock generator comprises:

a frequency divider for counting a clock signal and dividing the frequency of [[a]] the clock signal by N so as to output a frequency-divided clock signal;

a binarizer for receiving the wobble signal and for outputting a binary signal by comparing the wobble signal with a predetermined signal level,

a phase comparator for receiving the binary signal and detecting a phase difference between the binary signal and the output signal of the frequency divider so as to output a phase difference signal including information representing the phase difference;

a low pass filter for smoothing the phase difference signal;

a voltage-controlled oscillator for generating the clock signal, of which the frequency is determined by the output of the low pass filter, and outputting the clock signal to the frequency divider; ~~and~~

a time width detector for outputting a positive phase difference signal and a negative phase difference signal based on the phase difference signal; and

a phase shifter for advancing the count of the frequency divider if the amplitude of the positive phase difference signal is equal to or greater than a first predetermined value and delaying the count of the frequency divider if the amplitude of the negative phase difference signal is equal to or greater than a second predetermined value ~~controlling the frequency divider in accordance with the phase difference signal~~ so as to change the phase of the output signal of the frequency divider.

10. (Original) The optical disc drive of claim 9, wherein the wobbled tracks of the optical disc are modulated so as to represent address information.

11. (Currently amended) An optical disc controller being used for an optical disc drive and including the PLL clock generator for receiving an input signal and for generating an output signal, of which the frequency is N times (where N is a natural number equal to or greater than 1) as high as that of the input signal,

wherein the PLL clock generator comprises:

a frequency divider for counting a clock signal and dividing the frequency of [[a]] the clock signal by N so as to output a frequency-divided clock signal;

a phase comparator for receiving the input signal and detecting a phase difference between the input signal and the output signal of the frequency divider so as to output a phase difference signal including information representing the phase difference;

a low pass filter for smoothing the phase difference signal;

a voltage-controlled oscillator for generating the clock signal, of which the frequency is determined by the output of the low pass filter, and outputting the clock signal to the frequency divider; ~~and~~

a time width detector for outputting a positive phase difference signal and a negative phase difference signal based on the phase difference signal; and

a phase shifter for advancing the count of the frequency divider of the amplitude of the positive phase difference signal is equal to or greater than a first predetermined value and delaying the count of the frequency divider if the amplitude of the negative phase difference signal is equal to or greater than a second predetermined value ~~controlling the frequency divider in accordance with the phase difference signal~~ so as to change the phase of the output signal of the frequency divider.

12. (Currently amended) A method for controlling a PLL clock generator, the PLL clock generator receiving an input signal with a predetermined frequency and generating an output signal, of which the frequency is N times (where N is a natural number equal to or greater than 1) as high as the predetermined frequency,

wherein a first feedback loop is made up with a frequency divider for counting a clock signal and dividing the frequency of [[a]] the clock signal by N so as to output a frequency-divided clock signal; a phase comparator for receiving the input signal and detecting a phase

difference between the input signal and the output signal of the frequency divider so as to output a phase difference signal including information representing the phase difference; a low pass filter for smoothing the phase difference signal; and a voltage-controlled oscillator for generating the clock signal of which the frequency is determined by the output of the low pass filter, and outputting the clock signal to the frequency divider;

wherein a time width detector outputs a positive phase difference signal and a negative phase difference signal based on the phase difference signal,

wherein if the first feedback loop is under an asynchronous state, the method includes the step of controlling a phase shifter which advances the count of the frequency divider if the amplitude of the positive phase difference signal is equal to or greater than a first predetermined value and delays the count of the frequency divider if the amplitude of the negative phase difference signal is equal to or greater than a second predetermined value so as to change ~~controlling the frequency divider based on the phase difference signal and changing~~ the phase of the output signal of the frequency divider, whereby the frequency divider, the phase shifter and the phase comparator make up a second feedback loop.

13-14. (Canceled)